CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for testing a memory device comprising:

placing said memory device in a test mode;

resetting all match lines of said memory device;

enabling output from said match line under test;

decoding an address of a selected memory storage location corresponding to said match line under test;

loading said selected memory storage location with a known data pattern;

loading a comparand register with said known data pattern;

performing a search operation on said memory device; and

outputting a result of said search operation;

comparing said result of said search operation with an expected result of said search operation;

confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and

indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation.

2. The method according to claim 1, wherein said memory device is a content addressable memory (CAM) device.

3. The method according to claim 1, further comprising:

resetting output from said match line under test; and

enabling output from said memory storage location under test.

4. The method according to claim 1, wherein said resetting and said decoding acts occur on the rising edge of a clock signal.

5. The method according to claim 1, wherein said loading acts occur on the rising edge of a clock signal.

6. The method according to claim 1, wherein there is a one-to-one correspondence between said match lines and said memory storage locations.

7. The method according to claim 1, wherein there is a one-to-many correspondence between each said match line and said memory storage locations.

8. A method of testing a memory device that includes two or more sets of memory cells and, for each set of memory cells, a match line that provides a match signal when items of data stored in said set of memory cells satisfy a criterion, the method comprising:

enabling said match line of a set of memory cells being tested and disabling said match lines of other sets of memory cells;

applying said criterion to said items of data stored in the set of memory cells being tested, said stored items of data satisfying said criterion; and

receiving output signals from said match lines and determining whether said output signals indicate that said set of memory cells being tested has items of stored data that satisfy said criterion.

9. The method according to claim 8, in which said memory device is a content addressable memory (CAM) device.

10. The method according to claim 8, in which each set of memory cells is a memory storage location with an address and the act of determining includes determining whether said output signals indicate an address of said set of memory cells being tested.

11. The method according to claim 8, in which said criterion is whether said stored item of data matches a data item stored in a comparand register.

12. An apparatus for testing a match line of a memory device comprising:

a memory storage location corresponding to said match line under test, said match line under test further having a corresponding word line;

a comparator coupled to at least one search line per CAM memory cell of said memory storage location; and

a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal.

13. The apparatus according to claim 12, further comprising a priority encoder coupled to said circuit, said priority encoder outputting an address of said memory storage location corresponding to said match line under test if said match line under test is functioning properly.

14. The apparatus according to claim 12, wherein said memory device is a content addressable memory (CAM) device.

15. The apparatus according to claim 12, wherein there is a one-to-one correspondence between said match lines and said memory storage locations.

16. The apparatus according to claim 12, wherein there is a one-to-many correspondence between each said match line and said memory storage locations.

17. A memory circuit comprising:

a set of memory cells that store items of data;

comparison circuitry that applies a criterion to items of data stored in said set of memory cells and provides a match signal when said stored items of data satisfy said criterion; and

enabling circuitry that enables a match line to provide said match signal as output when said set of memory cells is being tested.

18. The memory circuit according to claim 17, in which said criterion is whether said stored item of data matches a data item stored in a comparand register.

19. The memory circuit according to claim 17, in which said set of memory cells stores said item of data, said memory circuit further comprising a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to said word line.

20. A memory device comprising:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that applies a criterion to items of data stored in said set of memory cells and provides a match signal when said stored items of data satisfy said criterion;

for each set of memory cells, enabling circuitry that enables a match line to provide said match signal as output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to said word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled.

21. The memory device according to claim 20, in which said memory device is a content addressable memory (CAM) device.

22. The memory device according to claim 20, in which each set of memory cells is a memory storage location with an address; the control circuitry determining whether said output signals indicate an address of said set of memory cells being tested.

23. A processing system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising circuitry for testing a match line of said CAM device, said CAM device further comprising:

a memory storage location corresponding to said match line under test, said match line under test further having a corresponding word line;

a comparator coupled to at least one search line per CAM memory cell of said memory storage location; and

a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal.

24. A method for testing a memory device comprising:

placing said memory device in a test mode;

resetting all match lines of said memory device;

enabling a match line under test;

decoding an address of a selected memory storage location corresponding to said match line under test;

loading said selected memory storage location with a known data pattern;

loading a comparand register with said known data pattern;

performing a search operation on said memory device;

outputting a result of said search operation;

comparing said result of said search operation with an expected result of said search operation;

confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and

indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation.

25. The method according to claim 24, wherein said memory device is a content addressable memory (CAM) device.

26. The method according to claim 24, wherein said resetting of all of said match lines and said decoding acts occur on the rising edge of a clock signal.

27. The method according to claim 24, wherein said loading acts occur on the rising edge of a clock signal.

28. The method according to claim 24, wherein there is a one-to-one correspondence between said match lines and said memory storage locations.

29. The method according to claim 24, wherein there is a one-to-many correspondence between each said match line and said memory storage locations.

30. An integrated circuit comprising:

a set of memory cells that store items of data;

comparison circuitry that applies a criterion to items of data stored in said set of memory cells and provides a match signal when said stored items of data satisfy said criterion; and

enabling circuitry that enables a match line to provide said match signal as output when said set of memory cells is being tested.

31. The integrated circuit according to claim 30, in which said criterion is whether said stored item of data matches a data item stored in a comparand register.

32. The integrated circuit according to claim 30, in which said set of memory cells stores said item of data, said memory circuit further comprising a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to said word line.

33. An integrated circuit comprising:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that applies a criterion to items of data stored in said set of memory cells and provides a match signal when said stored items of data satisfy said criterion;

for each set of memory cells, enabling circuitry that enables a match line to provide said match signal as output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to said word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled.

34. The integrated circuit according to claim 33, in which said memory device is a content addressable memory (CAM) device.

35. The integrated circuit according to claim 33, in which each set of memory cells is a memory storage location with an address and the control circuitry determines whether said output signals indicate an address of said set of memory cells being tested.

36. A router comprising:

a memory circuit that comprises:

a set of memory cells that store items of data;

comparison circuitry that applies a criterion to items of data stored in said set of memory cells and provides a match signal when said stored items of data satisfy said criterion; and

enabling circuitry that enables a match line to provide said match signal as output when said set of memory cells is being tested.

37. The router according to claim 36, in which said criterion is whether said stored item of data matches a data item stored in a comparand register.

38. The router according to claim 36, in which said set of memory cells stores said item of data, said memory circuit further comprising a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to said word line.

39. A router comprising:

a memory device that comprises:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that applies a criterion to items of data stored in said set of memory cells and provides a match signal when said stored items of data satisfy said criterion;

for each set of memory cells, enabling circuitry that enables a match line to provide said match signal as output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry enabling said match line in response to aid word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are enabled.

40. The router according to claim 36, in which said memory device is a content addressable memory (CAM) device.

41. The router according to claim 36, in which each set of memory cells is a memory storage location with an address and the control circuitry determines whether said output signals indicate an address of said set of memory cells being tested.

42. A system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for testing a match line of said CAM device, said apparatus further comprising:

a memory storage location corresponding to said match line under test, said match line under test further having a corresponding word line;

a comparator coupled to at least one search line per CAM memory cell of said memory storage location; and

a circuit coupled to said match line under test corresponding to said word line, and a test mode match line reset signal, wherein said circuit performs the following functions:

placing said memory device in a test mode;

resetting all match lines of said memory device;

enabling said match line under test;

decoding an address of a selected memory storage location corresponding to said match line under test;

loading said selected memory storage location with a known data pattern;

loading a comparand register with said known data pattern;

performing a search operation on said memory device; and

outputting a result of said search operation;

comparing said result of said search operation with an expected result of said search operation;

confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and

indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation.